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APPLICATION

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TITLE: RADIAL CONTACT PAD FOOTPRINT AND WIRING FOR ELECTRICAL COMPONENTS

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RADIAL CONTACT PAD FOOTPRINT AND WIRING FOR ELECTRICAL COMPONENTS

Background of the Invention

1. Technical Field

The present invention relates to a structure and associated method to wire an electrical device to a substrate.

2. Related Art

Typical electrical structures comprising electrical devices are limited in the amount of I/O connections that may be run from the electrical device to external connections on a substrate. Therefore any apparatus and method to allow more I/O connections to be run from an electrical device to external connections on a substrate would be welcome by the industry.

Summary of the Invention

The present invention provides an electrical structure, comprising:

contact pads on a surface of a substrate, wherein the contact pads are adapted to couple signal, power, and ground connections for an electrical device to a plurality of conductive wires on the substrate, wherein the contact pads are formed in single lines along radial edges of sectors on the substrate, wherein each sector comprises a predetermined angle between the radial edges of each of said sectors, wherein the sectors collectively form a circular area, and wherein the

contact pads comprise signal, power, and ground connections located at predetermined positions on the single lines along the radial edges of each of said sectors.

The present invention provides an electrical structure, comprising:

first contact pads on a surface of a substrate, wherein the first contact pads are adapted to couple signal, power, and ground connections for an electrical device to a first plurality of conductive wires on the substrate, wherein the first contact pads are formed in single lines along radial edges of sectors on the substrate, wherein each of the sectors comprise a predetermined angle between the radial edges of each of said sectors, wherein the sectors collectively form a quadrant in each corner of said substrate, and wherein the first contact pads comprise said signal, power, and ground connections located at predetermined positions on the single lines along the radial edges of the sectors within each quadrant; and

second contact pads on the surface of a substrate, wherein the second contact pads are adapted to couple signal, power, and ground connections for said electrical device to a second plurality of conductive wires on the substrate, wherein the second contacts pads are spaced apart a first predetermined distance in a first direction, wherein the second contact pads are spaced apart a second predetermined distance in a second direction, wherein first predetermined distance is different from said second predetermined distance, wherein the first direction is perpendicular to the second direction, and wherein the first and second contact pads are located on different areas on the substrate.

The present invention provides a method for forming an electrical structure, comprising:

forming contact pads on a surface of a substrate, wherein the contact pads are adapted to

couple signal, power, and ground connections for an electrical device to a plurality of conductive wires on the substrate, wherein the contact pads are formed in single lines along radial edges of sectors on the substrate, wherein each sector comprises a predetermined angle between the radial edges of each of said sectors, wherein the sectors collectively form a circular area, and wherein the contact pads comprise signal, power, and ground connections located at predetermined positions on the single lines along the radial edges of each of said sectors.

Brief Description of the Drawings

FIG. 1 is a plan view of an exemplary flip-chip module, in accordance with embodiments of the present invention.

FIG. 2 is a cross-sectional view through line 2-2 of the flip chip module of FIG. 1, in accordance with embodiments of the present invention.

FIG. 3 illustrates a top view of an electrical structure comprising an electrical device connected to contact pads on a substrate, in accordance with embodiments of the present invention.

FIG. 4 illustrates an alternative embodiment to FIG. 3 showing a top view of an electrical structure comprising an electrical device connected to two sets of contact pads on a substrate, in accordance with embodiments of the present invention.

FIG. 5 illustrates a top view of a reference mesh plane, in accordance with embodiments of the present invention.

FIG. 6 illustrates a top view of a solid reference plane comprising gas vent holes in accordance with embodiments of the present invention.

FIG. 7 illustrates an alternative embodiment to the reference mesh plane of FIG. 5 comprising a radial pattern and a dual pitch pattern for the contact pad footprint of FIG. 4, in accordance with embodiments of the present invention.

Detailed Description of the Invention

FIG. 1 is a top view of an exemplary flip-chip module. In FIG. 1, an integrated circuit chip **100** is flip-chip mounted to a module **105** having a multiplicity of pins **115**, in accordance with embodiments of the present invention. Each pin is electrically connected to a module contact pad **120** (see FIG. 2) by a conductive wire **125** within module **105**. Conductive wires may also be formed on top surface **110** of module **105**. Pins **115** may carry digital or analog signals, power or ground.

FIG. 2 is a cross-sectional view through line 2-2 of the flip chip module of FIG. 1, in accordance with embodiments of the present invention. FIG. 2 is at a larger scale than FIG. 1 in order to better illustrate the salient features of the interconnection between integrated circuit chip **100** and module **105**. In FIG. 2, module contact pads **120** are mechanically and electrically connected to chip contact pads **130** on a top surface **135** of integrated circuit chip **100** by solder bumps, solder balls or controlled collapse chip connections (C4). The name flip-chip module as applied to the combination of integrated circuit chip **100** and module **105** is readily apparent as integrated circuit chip **100** has been "flipped" upside down so the top surface **135** of the

integrated circuit chip is facing top surface **110** of module **105** in order to connect the integrated circuit chip **100** to the module.

While only one wiring layer is illustrated in FIGs. 1 and 2, the invention is applicable to modules having multiple wiring layers. For example, with two wiring layers, escaping wires in a second wiring layer would be positioned under the escaping wires of the first layer between columns of module contact pads. Alternatively, the first wiring layer may be on the surface of the module and the second wiring layer within the module. However, the invention reduces the number of wiring layers that would be required in a module from the number that would otherwise be required without the present invention as described *infra*. It should also be noted that while a pin grid array module has been illustrated in FIGs. 1 and 2, the present invention is applicable to other types of modules such as ball grid arrays, solder column grid arrays and land grid arrays.

Further, it should be noted that modules constitute only one type of substrate to which the present invention is applicable. Other types of substrates include but are not limited to, single wiring layer or multi-layer wiring layer integrated circuit chip modules, single wiring layer or multi-layer wiring layer printed circuit boards, single wiring layer or multi-layer wiring layer flexible circuit boards, single wiring layer or multi-layer wiring layer interposers, single wiring layer or multi-layer wiring layer ceramic substrates, single wiring layer or multi-layer wiring layer organic substrates and integrated circuit chips.

Contact pads and wires interconnecting contact pads may be formed by any number of methods well known in the art.

FIG. 3 illustrates an alternative embodiment to FIG 1 and 2 showing a top view of an electrical structure **4** comprising an electrical device **15** connected to contact pads **12** on a substrate (organic, ceramic, etc) **10** in accordance with embodiments of the present invention. The contact pads **12** create a radial contact pad footprint on the substrate **10**. The electronic structure **4** may include, *inter alia,* a flip chip plastic ball grid array module (FC-PBGA), an organic chip carrier, a ceramic chip carrier, etc. The electrical device **15** may be any electrical device known to a person of ordinary skill in the art such as, *inter alia,* a semiconductor chip. Alternatively the electrical device **15** may be, *inter alia*, a chip carrier with an attached semiconductor chip, an interposer with an attached semiconductor chip, etc. The electrical device **15** is electrically connected to the substrate **10** using an electrical connector (e.g., a Controlled Collapse Chip Connection (C4) solder ball). The substrate **10** may comprise, *inter alia*, a chip carrier (e.g., an organic chip carrier, a ceramic chip carrier, etc.) or a printed circuit board (e.g., an organic printed circuit board , a ceramic printed circuit board, etc.). The contact pads **12** may be adapted to connect signal, such as input/output (I/O), power, and ground connections for the electrical device **15**, to a plurality of conductive wires **8** on the substrate **10**. The plurality of conductive wires **8** on the substrate **10** are adapted to carry I/O, power, and ground signals to and from the electrical device **15** from an outside source such as, *inter alia*, a power supply/source, an electrical device, a microprocessor, etc. The I/O, power, and ground signals may be analog or digital signals. The contact pads **12** are arranged on the substrate **10** in a radial pattern such that contact pads **12** are formed on radial edges **17** of sectors **18** on the substrate **10**. Each of the sectors **18** comprise a predetermined angle **22** between the radial edges

17 of each of the sectors **18**. The sectors **18** in combination form a circular area **25** on the substrate **10**. The contact pads **12** may comprise signal, power, and ground pads located at predetermined positions along the radial edges **17** of the sectors **18** on the substrate **10**. The plurality of conductive wires **8** on the substrate **10** are positioned between the radial edges **17** of the sectors **18** on the substrate **10**. The radial arrangement of the contact pads **12** provides an increasing amount of space between the contact pads **12** along the radial edges **17** of the sectors **18** as the contact pads **8** are positioned closer to the outer circumference of the circular area **25**. Each predetermined angle **22** may be determined based on the number of conductive wires **8** positioned between the radial edges **17** of the sectors **18**, the width of each of the conductive wires **8**, and the space required between each adjacent conductive wire. The contact pads **12** may be adapted for solder bump, solder ball, or controlled collapse chip connection attachment to the electrical device **15**. The substrate **10** may comprise a single wiring layer or a multi-layer wiring layer integrated circuit chip module, a single wiring layer or a multi-layer wiring layer printed circuit board, a single wiring layer or multi-layer wiring layer flexible circuit board, a single wiring layer or a multi-layer wiring layer interposer, a single wiring layer or a multi-layer wiring layer ceramic substrate, a single wiring layer or a multi-layer wiring layer organic substrate. Further, it should be readily apparent that the contact pad footprint on electrical device **15** is a mirror image of the corresponding contact pad footprint of the substrate **10**, so when the electrical device **15** footprint is described, the description is applicable to the corresponding contact pad footprint of the substrate **10** and vice versa.

FIG. 4 illustrates an alternative embodiment to FIG. 3 showing a top view of an electrical

structure **30** comprising an electrical device **42** connected to contact pads **34** in corner sections **50** and contact pads **38** in sections **54** on a substrate **40** (organic, ceramic, etc) in accordance with embodiments of the present invention. The contact pads **34** and the contact pads **38** together create a contact pad footprint on the substrate **40**. The electronic structure **30** may include, *inter alia,* a flip chip plastic ball grid array module (FC-PBGA), an organic chip carrier, a ceramic chip carrier, etc. The electrical device **42** may be any electrical device known to a person of ordinary skill in the art such as, *inter alia,* a semiconductor chip. Alternatively, the electrical device **42** may be, *inter alia*, a chip carrier with an attached semiconductor chip, an interposer with an attached semiconductor chip, etc. The electrical device **42** may be electrically connected to the substrate **40** using an electrical connector (e.g., a Controlled Collapse Chip Connection (C4) solder ball). The substrate **40** may comprise, *inter alia*, a chip carrier (e.g., an organic chip carrier, a ceramic chip carrier, etc.) or a printed circuit board (e.g., an organic printed circuit board , a ceramic printed circuit board, etc.). The contact pads **34** and the contact pads **38** are adapted to connect signal, such as (I/O), power, and ground connections for the electrical device **42**, to a plurality of conductive wires **46** and **37** on the substrate **40**. The plurality of conductive wires **46** and **37** on the substrate **40** are adapted to carry I/O, power, and ground signals to and from the electrical device **42** from an outside source such as, *inter alia*, a power supply/source, an electrical device, a microprocessor, etc. The I/O, power, and ground signals may be analog or digital signals. The contact pads **34** on the substrate **40** are located in each of the four corner sections **50** of the substrate **40** and comprise the radial pattern of FIG. 3, thereby allowing a maximum amount of the conductive wires **46** to run from the contact pads **34** to external

connections on the substrate **40**. In contrast with FIG. 3, the radial pattern of FIG. 4 is only located in the four corner sections **50** of the substrate **40**. Note that all other features of the contact pads **34** comprising the radial pattern are the same as the radial pattern if FIG. 3 as described *supra*. The contact pads **38** located in the sections **54** of the substrate **40** each comprise a dual pitch pattern. The dual pitch pattern places each of the contact pads **38** located in sections **54** a first predetermined distance **44** from each other in a first direction and a second predetermined distance **45** from each other in a second direction. The first predetermined distance **44** is different from the second predetermined distance **45**. The first direction is perpendicular to the second direction in each of the four sections **54** of the substrate. A plurality of conductive wires **37** on the substrate **40** are positioned between adjacent contact pads, spaced apart by the first predetermined distance **44**. The first predetermined distance **44** is calculated based on the number of conductive wires positioned between the adjacent contact pads in said first direction, the width of each of said conductive wires, and the space required between each adjacent conductive wire. The substrate **40** may comprise a single wiring layer or a multi-layer wiring layer integrated circuit chip module, a single wiring layer or a multi-layer wiring layer printed circuit board, a single wiring layer or a multi-layer wiring layer flexible circuit board, a single wiring layer or a multi-layer wiring layer interposer, a single wiring layer or a multi-layer wiring layer ceramic substrate, a single wiring layer or a multi-layer wiring layer organic substrate. Further, it should be readily apparent that the contact pad footprint on electrical device **42** is a mirror image of the corresponding contact pad footprint of the substrate **40**, so when the electrical device **42** footprint is described, the description is applicable to the corresponding

contact pad footprint of the substrate **40** and vice versa.

FIG. 5 illustrates a top view of a substrate **10** including a reference mesh plane **72** comprising a radial pattern in accordance with embodiments of the present invention. A reference mesh plane comprises a plurality of reference conductors used to carry return currents from signal wires (e.g, see wires **8** of FIG. 3 and wires **37** and **46** of FIG. 4) back to a signal source. A reference conductor should be placed in close proximity to each signal wire to minimize crosstalk between each of the signal wires and insure signal integrity. A multilayer substrate (organic, ceramic, etc) may be used with the reference mesh plane **72** so that the signal wires may be placed on a first layer and the reference mesh plane **72** may be placed on a second layer above or a third layer below the signal wires. Alternatively, the reference mesh plane **72** may be placed on the second layer above and the third layer below the signal wires. A reference mesh plane comprises one potential such as, *inter alia*, power, ground, etc. A reference mesh plane may be used with any contact pad footprint of a substrate including the contact pad footprints of FIGS. 3 and 4. For the contact pad footprint of FIG. 3, the reference mesh plane **72** of FIG. 5 may be used in accordance with embodiments of the present invention. Similarly, fro the contact pad footprint of FIG. 4, the reference mesh plane **84** of FIG. 7 may be used. The reference mesh plane **72** comprises a first group of electrically conductive wires **75** and a second group of electrically conductive wires **76**. The first group of electrically conductive wires **75** are formed in a first pattern comprising concentric circles. The second group of electrically conductive wires **76** are formed in a second pattern comprising single lines lying on radii of the concentric circles. The first group of electrically conductive wires **75** are electrically connected

to the second group of electrically conductive wires **76**, thereby forming a grid. Each of the wires **8** of FIG. 3 may be run coincidence with each of the electrically conductive wires **76** but on separate adjacent vertical layers. Therefore, each of the wires **8** has it's own electrically conductive wire **76** to carry return currents thereby reducing electrical noise and preserving signal integrity.

FIG. 6 illustrates a top view of a substrate **10** including an electrical device **10** and a solid reference plane **78** comprising a radial pattern of gas vent holes **80** in accordance with embodiments of the present invention. As with the reference mesh plane **72** of FIG. 5, the solid reference plane **78** is used to carry return currents from signal wires (e.g, see wires **8** of FIG. 3 and wires **37** of FIG. 4) back to a signal source. In contrast to the reference mesh plane **72** of FIG. 5, the solid reference plane **78** comprises a solid metal reference conductor instead of a conductive grid. A multilayer substrate (organic, ceramic, etc) may be used with the solid reference plane **78** so that the signal wires may be placed on a first layer and the solid reference plane may be placed on a second layer above or below the signal wires. Alternatively, the solid reference plane **78** may be placed on the second layer above and the third layer below the signal wires. The solid reference plane**78** comprises one potential such as, *inter alia*, power, ground, etc. The solid reference plane **78** may be used with any contact pad footprint of a substrate including the contact pad footprints of FIGS. 3 and 4. The solid reference plane **78** includes a pattern of holes or openings called gas vent holes **80**. The gas vent holes **80** are used to vent or release gasses formed during fabrication of dielectric laminate substrates to insure a proper lamination of layers. "Lamination" of layers, etc is defined herein as adhesively stacking said

layers, etc in any manner known to one of ordinary skill in the art. The gas vent holes **80** are placed in a location in the solid reference plane **78** such that the electrically conductive wires **8** of FIG. 3 and the electrically conductive wires **46** and **37** of FIG. 4 are not located above or below the gas vent holes **80**. In reference to FIG. 3, the gas vent holes **80** may form the same pattern as the wires **8** but offset to the right or left. In reference to FIG. 4, the gas vent holes **80** may form the same pattern as the wires **46**and **37** but offset to the right or left.

FIG. 7 illustrates an alternative embodiment to the reference mesh plane **72** of FIG. 5 showing a top view of a substrate **41** including a reference mesh plane **84** comprising a radial pattern and a dual pitch pattern for the contact pad footprint of FIG. 4, in accordance with embodiments of the present invention. In contrast with the reference mesh plane **72** of FIG. 5, the reference mesh plane **84** comprises a similar pattern as a pattern formed by the wires **37** and **45** of FIG. 4. The reference mesh plane **84** comprises a first group of electrically conductive wires **87** and a second group of electrically conductive wires **86**. The first group of electrically conductive wires **87** are formed in a first pattern comprising concentric shapes (e.g., an oval shape) . The second group of electrically conductive wires **86** are formed in a second pattern comprising single lines lying on radii of the concentric oval shapes. The first group of electrically conductive wires **87** are electrically connected to the second group of electrically conductive wires **86**, thereby forming a grid. Each of the wires **46** and **37** of FIG. 4 may be run coincidence with each of the electrically conductive wires **86** but on separate adjacent vertical layers. Therefore, each of the wires **46** and **37** of FIG. 4 has it's own electrically conductive wire **86** to carry return currents, thereby reducing electrical noise and preserving signal integrity.

While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.